PRELIMINARY AMENDEMENT

Amendments to the Claims:

Please amend claims 10 and 26. The claims are as follows:

Listing of Claims:

1. (Original) An electronic device, comprising:

an interlevel dielectric layer formed on a semiconductor substrate;

a copper bottom electrode formed in said interlevel dielectric layer, a top surface of said bottom electrode co-planer with a top surface of said interlevel dielectric layer;

a conductive diffusion barrier in direct contact with said top surface of said bottom electrode;

a MIM dielectric in direct contact with a top surface of said conductive diffusion barrier; and

a top electrode in direct contact with a top surface of said MIM dielectric.

2. (Original) The electronic device of claim 1, wherein said conductive diffusion barrier and said MIM dielectric both extend past at least two sides of said bottom electrode.

3. (Original) The electronic device of claim 1, further including:

a dielectric diffusion barrier layer formed on said top surface of said interlevel dielectric layer; and

wherein said top surface of said conductive diffusion barrier is co-planer with a top surface of said dielectric diffusion barrier layer.

4. (Original) The electronic device of claim 1, wherein said bottom electrode includes an upper portion comprising an additional conductive diffusion barrier, said upper portion in contact with said conductive diffusion barrier.

5. (Original) The electronic device of claim 4, wherein said additional conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

6. (Original) The electronic device of claim 1, wherein said conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

7. (Original) The electronic device of claim 1, wherein said MIM dielectric comprises about 2 to 20 nm of SiO_2, Si_3N_4 or SiC, a high K dielectric, Ta_2O_5, $BaTiO_3$, HfO_2, ZrO_2 or Al_2O_3, or combinations of layers thereof.

8. (Original) The electronic device of claim 1, wherein said top electrode comprises Al or W.

9. (Original) An electronic device, comprising:

an interlevel dielectric layer formed on a semiconductor substrate;

a copper bottom electrode formed in said interlevel dielectric layer;

a conductive diffusion barrier in direct contact with a top surface of said bottom electrode, said top surface of said bottom electrode recessed below a top surface of said interlevel dielectric layer, said top surface of said conductive diffusion barrier co-planer with said top surface of said interlevel dielectric layer;

a MIM dielectric in direct contact with a top surface of said conductive diffusion barrier; and

a top electrode in direct contact with a top surface of said MIM dielectric.

10. (Currently Amended) The electronic device of claim 9, wherein ~~said conductive diffusion barrier and~~ said MIM dielectric ~~both~~ extends past at least two sides of said bottom electrode.

11. (Original) The electronic device of claim 9, wherein said conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

12. (Original) The electronic device of claim 9, wherein said MIM dielectric comprises about 2 to 20 nm of SiO_2, Si_3N_4 or SiC, a high K dielectric, Ta_2O_5, $BaTiO_3$, HfO_2, ZrO_2 or Al_2O_3, or combinations thereof.

13. (Original) The electronic device of claim 9, wherein said top electrode comprises Al or W.

14. (Original) A method of fabricating an electronic device, comprising:

(a) providing a semiconductor substrate

(b) forming an interlevel dielectric layer on said semiconductor substrate;

(c) forming a copper bottom electrode in said interlevel dielectric layer, a top surface of said bottom electrode co-planer with a top surface of said interlevel dielectric layer;

(d) forming a conductive diffusion barrier in direct contact with said top surface of said bottom electrode;

(e) forming a MIM dielectric in direct contact with a top surface of said conductive diffusion barrier; and

(f) forming a top electrode in direct contact with a top surface of said MIM dielectric.

15. (Original) The method of claim 14, wherein said conductive diffusion barrier and said MIM dielectric both extend past at least two sides of said bottom electrode.

16. (Original) The method of claim 14, further including:

(g) after step (c) forming a dielectric diffusion barrier layer on said top surface of said interlevel dielectric layer; and

wherein said top surface of said conductive diffusion barrier is co-planer with a top surface of said dielectric diffusion barrier layer.

17. (Original) The method of claim 14, wherein said bottom electrode includes an upper portion comprising an additional conductive diffusion barrier, said upper portion in contact with said conductive diffusion barrier.

18. (Original) The method of claim 17, wherein said additional conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

19. (Original) The method of claim 14, wherein said conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

20. (Original) The method of claim 1, wherein said MIM dielectric comprises about 2 to 20 nm of SiO_2, Si_3N_4 or SiC, a high K dielectric, Ta_2O_5, $BaTiO_3$, HfO_2, ZrO_2 or Al_2O_3, or combinations thereof.

21. (Original) The method of claim 14, wherein said top electrode comprises Al or W.

22. (Original) The method of claim 14, wherein step (d) further comprises simultaneously forming a resistor, an alignment mark or both a resistor and an alignment mark with said conductive diffusion barrier.

23. (Original) The method of claim 22, wherein said resistor, said alignment mark or both said resistor and said alignment mark comprise about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations of layers thereof.

24. (Original) The method of claim 14, further including (g) after step (f) depositing a reactive ion etch layer over all exposed surfaces of said conductive diffusion barrier, said MIM dielectric and said interlevel dielectric layer.

25. (Original) A method of fabricating an electronic device, comprising:

(a) providing a semiconductor substrate;

(b) forming an interlevel dielectric layer on said semiconductor substrate;

(c) forming a copper bottom electrode in said interlevel dielectric layer;

(d) forming a conductive diffusion barrier in direct contact with a top surface of said bottom electrode, said top surface of said bottom electrode recessed below a top surface of said interlevel dielectric layer, said top surface of said conductive diffusion barrier co-planer with said top surface of said interlevel dielectric;

(e) forming a MIM dielectric in direct contact with said top surface of said conductive diffusion barrier; and

(f) forming a top electrode in direct contact with a top surface of said MIM dielectric.

26. (Currently Amended) The method of claim 25, wherein ~~said conductive diffusion barrier and~~ said MIM dielectric ~~both~~ extends past at least two sides of said bottom electrode.

27. (Original) The method of claim 25, wherein said conductive diffusion barrier comprises about 5 to 200 nm of a refractory metal, W, Ta, TaN, WN, TaN, TaSiN, Pt, IrO_2 or RuO_2 or combinations thereof.

28. (Original) The method of claim 25, wherein said MIM dielectric comprises about 2 to 20 nm of SiO_2, Si_3N_4 or SiC, a high K dielectric, Ta_2O_5, $BaTiO_3$, HfO_2, ZrO_2 or Al_2O_3, or combinations thereof.

29. (Original) The method of claim 25, wherein said top electrode comprises Al or W.

30. (Original) The method of claim 25, further including (g) after step (f) depositing a reactive ion etch layer over all exposed surfaces of said conductive diffusion barrier, said MIM dielectric and said interlevel dielectric layer